CLAIMS

1. A memory controller for controlling a memory having a plurality of banks, comprising:

an arbitration circuit for arbitrating a memory access request for making access to the memory from a plurality of blocks,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory, and

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access, wherein

priority of memory access from the plurality of blocks is changed so as to make access to a different bank from memory access having been permitted by the arbitration circuit immediately before.

2. The memory controller according to claim 1, wherein the arbitration circuit comprises:

a request receiving block which receives a memory request and a memory address from the plurality of blocks, includes a bank decision unit for deciding whether access is made to the same bank based on the received memory address, and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating the priority of memory access from the plurality of blocks,

an identical bank priority designating unit for selecting a block to be subsequently permitted to access when a memory access request is made from the plurality of blocks to the same bank as immediately preceding access,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

3. The memory controller according to claim 1, wherein the arbitration circuit lowers the priority of memory access made from the block to the same bank as memory access having been permitted immediately before.

4. The memory controller according to claim 1, wherein the arbitration circuit increases the priority of memory access made from the block to a bank different from memory access having been permitted immediately before.

5. The memory controller according to claim 1, wherein the arbitration circuit lowers the priority of memory access when the bank where memory access is permitted immediately before is the same as a subsequent memory access request.

6. The memory controller according to claim 2, wherein the memory access priority designating unit can be set from outside and priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

7. The memory controller according to claim 2, wherein the identical bank priority designating unit can be set from outside and a block to be subsequently permitted to access the memory can be selected according to priority set by the identical bank priority designating unit when a memory access

request is made from the plurality of blocks to the same bank as immediately preceding access.

8. The memory controller according to claim 1, wherein the memory is a synchronous memory.

9. A memory controller for controlling a memory having a plurality of banks, comprising:

an arbitration circuit for arbitrating a memory access request for making access to the memory from a plurality of blocks,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory, and

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access, wherein

bank access data is access data to the memory, the access data having a predetermined number of bytes for performing writing or reading on the same bank of the memory, block access data is a data unit constituted of two sets of the bank access data belonging to different banks, and in the case where the plurality of blocks make a memory access request for each piece of the block access data, when a second-half bank where memory access is permitted immediately before is the same as the first-half bank of a subsequent memory access request, the arbitration circuit changes an order of memory access of the bank access data in the block access data.

10. The memory controller according to claim 9, wherein the arbitration circuit comprises:

a request receiving block which receives a memory request and a memory address from the plurality of blocks, includes a bank decision unit for deciding, based on the received memory address, whether access is made to the same bank regarding a second-half bank where memory access has been permitted immediately before and a first-half bank of a subsequent memory access request, and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating priority of memory access from the plurality of blocks,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

11. The memory controller according to claim 9, wherein the data latch block comprises:

a write data latch block which receives and latches write data from the plurality of blocks,

a data change block which, based on a data latch control signal from the arbitration circuit, changes an order of bank access data outputted by the write data latch block, outputs the data as write data to the memory, changes an order of bank access data outputted by a read data latch block (described later), and outputs the data as read data to a block permitted to perform read access to the memory, and

a read data latch block which receives and latches the read data having been read from the memory.

12. The memory controller according to claim 9, wherein when the second-half bank where memory access has been permitted immediately before is the same as the first-half bank of the

subsequent memory access request, the arbitration circuit changes an order of the bank access data in the block access data, reads the block access data from the memory, and stores the data in the data latch block, and the data latch block changes an order of each piece of the bank access data in the block access data and transfers the data to the block having performed memory access.

13. The memory controller according to claim 10, wherein the memory access priority designating unit can be set from outside and the priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

14. The memory controller according to claim 9, wherein the memory is a synchronous memory.

15. A memory controller for controlling a memory having a plurality of banks, comprising:

an arbitration circuit for arbitrating a memory access request for making access to the memory from a plurality of blocks,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory, and

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access, wherein

when bank access data is access data to the memory, the access data having a predetermined number of bytes for performing writing or reading on the same bank of the memory,

and block access data is a data unit constituted of two sets of the bank access data belonging to different banks, the arbitration circuit instructs the command generation block to provide a wait cycle when a memory access request is made by the bank access data alone from the block permitted to access the memory.

16. The memory controller according to claim 15, wherein the arbitration circuit comprises:

a request receiving block which receives a memory request from the plurality of blocks, includes a data unit decision unit for deciding a data unit of requested memory access based on the received memory request, and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating priority of memory access from the plurality of blocks,

a wait cycle designating unit for designating the number of wait cycles provided when memory access is requested from the plurality of blocks by the bank access data alone,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

17. The memory controller according to claim 16, wherein the memory access priority designating unit can be set from outside and the priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

18. The memory controller according to claim 16, wherein the wait cycle designating unit can be set from outside and the

number of wait cycles provided by the command generation block can be changed according to a setting of the wait cycle designating unit.

19. The memory controller according to claim 15, wherein the memory is a synchronous memory.

20. A memory controller for controlling a memory having a plurality of banks, comprising:

an arbitration circuit for arbitrating a memory access request for making access to the memory from a plurality of blocks,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory, and

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access, wherein

when memory access permitted by the arbitration circuit immediately before is read access, priority of a memory access requests from the plurality of blocks is changed so as to successively perform read access.

21. The memory controller according to claim 20, wherein the arbitration circuit comprises:

a request receiving block which receives a memory request from the plurality of blocks, includes an access request decision unit for deciding the kind of requested memory access based on the received memory request, and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating priority of memory access from the plurality of blocks,

a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when memory access permitted immediately before is read access,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

22. The memory controller according to claim 20, wherein the arbitration circuit increases priority of read access when memory access permitted immediately before is read access.

23. The memory controller according to claim 20, wherein the arbitration circuit increases priority of read access when memory access permitted immediately before is read access and a subsequent memory access is made for read access.

24. The memory controller according to claim 21, wherein the memory access priority designating unit can be set from outside and the priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

25. The memory controller according to claim 20, wherein the read access priority designating unit can be set from outside and a block to be subsequently permitted to perform read access to the memory can be selected according to priority set by the read access priority designating unit when memory access

permitted by the arbitration circuit immediately before is read access.

26. The memory controller according to claim 20, wherein the memory is a synchronous memory.

27. A memory controller for controlling a memory having a plurality of banks, comprising:

a refresh request block for requesting refresh at a regular interval to store the internal data of the memory,

an arbitration circuit for arbitrating a memory access request for accessing the memory from a plurality of blocks and a refresh request from the refresh request block,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory, and

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access, wherein

when memory access permitted by the arbitration circuit immediately before is write access, priority of a refresh request from the refresh request block is changed.

28. The memory controller according to claim 27, wherein the arbitration circuit comprises:

a request receiving block which receives the refresh request from the refresh request block and the memory request from the plurality of blocks, includes an access request decision unit for deciding the kind of requested memory access based on the received refresh request and memory request, and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating priority of memory access from the plurality of blocks,

a write access priority designating unit for selecting a block to be subsequently permitted to perform read access when the refresh request is outputted from the refresh request block and memory access permitted by the arbitration circuit immediately before is write access,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

29. The memory controller according to claim 27, wherein the arbitration circuit lowers the priority of a refresh request when memory access permitted immediately before is write access.

30. The memory controller according to claim 27, wherein the arbitration circuit lowers the priority of a refresh request when memory access permitted immediately before is write access and a subsequent memory access request includes a refresh request.

31. The memory controller according to claim 28, wherein the memory access priority designating unit can be set from outside and the priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

32. The memory controller according to claim 28, wherein the write access priority order designating unit can be set from outside and a block to be subsequently permitted to access

the memory can be selected according to priority set by the write access priority order designating unit when a refresh request is outputted from the refresh request block and memory access permitted by the arbitration circuit immediately before is write access.

33. The memory controller according to claim 27, wherein the memory is a synchronous memory.

34. A memory controller for controlling a memory having a plurality of banks, comprising:

an arbitration circuit for arbitrating a memory access request for making access to the memory from a plurality of blocks,

a command generation block for generating a memory command for the memory based on a control signal from the arbitration circuit,

an address generation block which receives a memory address from the block permitted to access by the arbitration circuit and outputs the memory address to the memory,

a data latch block which latches write data from the block permitted to access by the arbitration circuit or read data from the memory and passes data between the memory and the block permitted to access,

wherein the arbitration circuit designates an arbitrating method for changing priority of memory access from the plurality of blocks when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access.

35. The memory controller according to claim 34, wherein the arbitration circuit comprises:

a bank decision unit which receives a memory address from the plurality of blocks and decides whether access is made to the same bank or not based on the received memory address,

an access request decision unit which receives a memory request from the plurality of blocks and decides the kind of requested memory access based on the received memory request,

a request receiving block which includes the bank decision unit and the access request decision unit and provides an instruction to generate an enabling signal,

a memory access priority designating unit for designating the priority of memory access from the plurality of blocks,

an arbitrating method designating unit for designating an arbitrating method for changing the priority of memory access when the memory access request from the plurality of blocks is made to the same bank as immediately preceding access and memory access permitted by the arbitration circuit immediately before is read access,

an identical bank priority designating unit for selecting a block to be subsequently permitted to access when the arbitrating method designating unit is set so as to place higher priority on a bank,

a read access priority designating unit for selecting a block to be subsequently permitted to perform read access when the arbitrating method designating unit is set so as to place higher priority on access,

an enabling signal generation block which is instructed by the request receiving block to generate the enabling signal and outputs the enabling signal to the block permitted to access the memory, and

a control signal generation block which is instructed by the request receiving block to generate the control signal and generates each control signal.

36. The memory controller according to claim 35, wherein the memory access priority designating unit can be set from outside

and the priority of access from the plurality of blocks to the memory can be changed according to a setting of the memory access priority designating unit.

37. The memory controller according to claim 35, wherein the arbitrating method designating unit can be set from outside and the arbitrating method of memory access from the plurality of blocks can be changed according to a setting of the arbitrating method designating unit.

38. The memory controller according to claim 35, wherein the identical bank priority designating unit can be set from outside and a block to be subsequently permitted to access to the memory can be selected according to priority set by the identical bank priority designating unit when the arbitrating method designating unit is set so as to place higher priority on a bank and a memory access request is made from the plurality of blocks to the same bank as immediately preceding access.

39. The memory controller according to claim 35, wherein the read access priority designating unit can be set from outside and a block to be subsequently permitted to perform read access to the memory can be selected according to priority set by the read access priority designating unit when the arbitrating method designating unit is set so as to place higher priority on access and memory access permitted by the arbitration circuit immediately before is read access.

40. The memory controller according to claim 34, the memory is a synchronous memory.